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1   Time synch and localization: Asymptotically optimal time synchronization in dense sensor networks   ▬
An-swol Hu, Sergio D. Servetto
September 2003 **Proceedings of the 2nd ACM international conference on Wireless sensor networks and applications**
Full text available: 📄 pdf(195.22 KB)   Additional Information: full citation, abstract, references, index terms

We consider the problem of synchronization of all clocks in a sensor network, in the regime of asymptotically high node densities. We formulate this problem as one in which all clocks must line up with the clock of an arbitrary node in the network (of course *without* assuming that this clock can be observed everywhere in the network, nor assuming that this node has any special hardware--this node could be any). We give a state-space description for the generation of observable data as a fu ...

2   Special issue on wireless pan & sensor networks: TSync: a lightweight bidirectional time synchronization service for wireless sensor networks   ▬
Hui Dai, Richard Han
January 2004 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 8 Issue 1
Full text available: 📄 pdf(453.89 KB)   Additional Information: full citation, abstract, references

Time synchronization in a wireless sensor network is critical for accurate timestamping of events and fine-tuned coordination of wake/sleep duty cycles to reduce power consumption. This paper proposes TSync, a novel lightweight bidirectional time synchronization service for wireless sensor networks. TSync's bidirectional service offers both a push mechanism for accurate and low overhead global time synchronization as well as a pull mechanism for on-demand synchronization by individual sensor nod ...

3   Physical interface: Fine-grained network time synchronization using reference broadcasts   ▬
Jeremy Elson, Lewis Girod, Deborah Estrin
December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI
Full text available: 📄 pdf(2.10 MB)   Additional Information: full citation, abstract, references, citings

Recent advances in miniaturization and low-cost, low-power design have led to active research in large-scale networks of small, wireless, low-power sensors and actuators. Time synchronization is critical in sensor networks for diverse purposes including sensor data fusion, coordinated actuation, and power-efficient duty cycling. Though the clock accuracy and precision requirements are often stricter than in traditional distributed systems, strict energy constraints limit the resources available ...

4 Design of half-rate clock and data recovery circuits for optical communication systems

Jafar Savoj, Behzad Razavi

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(1.78 MB)   Additional Information: full citation, abstract, references, index terms

This paper describes the design of two half-rate clock and data recovery circuits for optical receivers. Targeting the data rate of 10-Gb/s, the first implementation incorporates a ring oscillator and a linear phase detector whereas the second implementation uses a multiphase LC oscillator and a bang-bang phase/frequency detector. Fabricated in 0.18-&mgr;m CMOS technology, the power consumption of each of the circuits is less than 100~mW. The rms jitter of the output clock for the tw ...

5 Multipoint audio and video control for packet-based multimedia conferencing

F. Gong

October 1994 **Proceedings of the second ACM international conference on Multimedia**

Full text available: pdf(979.60 KB)   Additional Information: full citation, abstract, references, citings, index terms

With the advent of broadband integrated services data network (B-ISDN) technologies such as Asynchronous Transfer Mode (ATM) networks, packet-based multimedia (e.g., live audio and video, animation, and text) conferencing is becoming a viable means for achieving virtual proximity, which enables us to overcome the physical separation in space and time and to interact more effectively in our science and engineering endeavors. To bring about the reality of virtual proximity, many technical iss ...

6 Mixed analog-digital design: Digital background and blind calibration for clock skew error in time-interleaved analog-to-digital converters

David Camarero, Jean-François Naviner, Patrick Loumeau

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(146.26 KB)   Additional Information: full citation, abstract, references, index terms

This paper deals with the problem of clock skew errors in time-interleaved analog-to-digital converters. Deterministic sample-time errors between time-interleaved channels generate nonlinear distortion and degrade SFDR. We propose a fully digital calibration method that uses, on the one hand, adaptive FIR filters to reconstruct a correctly sampled signal and, on the other hand, a new blind clock skew detection algorithm that guides the adaptive filters. This calibration method applies to any num ...

Keywords: adaptive filters, clock skew, digital calibration, parallel ADC, sample-time errors, time-interleaved

7 Energy aware design: Dynamic frequency and voltage control for a multiple clock domain microarchitecture

Greg Semeraro, David H. Albonesi, Steven G. Dropsho, Grigorios Magklis, Sandhya Dwarkadas, Michael L. Scott

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.17 MB) Publisher Site   Additional Information: full citation, abstract, references, citings, index terms

We describe the design, analysis, and performance of an on--line algorithm to dynamically control the frequency/voltage of a Multiple Clock Domain (MCD) microarchitecture. The MCD microarchitecture allows the frequency/voltage of microprocessor regions to be adjusted independently and dynamically, allowing energy savings when the frequency of some regions can be reduced without significantly impacting performance.Our algorithm achieves on average a 19.0% reduction in Energy Per Instruction (EPI) ...

8 Low-level multimedia synchronization algorithms on broadband networks

Miguel Correia, Paulo Pinto
January 1995 **Proceedings of the third ACM international conference on Multimedia**
Full text available: ⬚ html(59.69 KB)   Additional Information: full citation, references, index terms

Keywords: broadband networks, distributed multimedia systems, low-level synchronization

9 Synchronization in multimedia data retrieval
Anna Haj Haċ, Cindy X. Xue
January 1997 **International Journal of Network Management**, Volume 7 Issue 1

Full text available: ⬚ pdf(487.64 KB)   Additional Information: full citation, abstract, references, index terms

Synchronization of multiple medium streams in real time has been recognized as one of the most important requirements for multimedia applications based on broadband high-speed networks. This article presents a complete synchronization scheme for distributed multimedia information systems. © 1997 John Wiley & Sons, Ltd.

10 VLSI circuits: A globally asynchronous locally dynamic system for ASICs and SoCs
Atanu Chattopadhyay, Zeljko Zilic
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**

Full text available: ⬚ pdf(545.50 KB)   Additional Information: full citation, abstract, references, index terms

An architecture that combines a Globally Asynchronous, Locally Synchronous (GALS) [1,2] design style with dynamic voltage and frequency scaling can use the slowest frequency possible to accomplish a task with minimum power consumption. The proposed Globally Asynchronous, Locally Dynamic System (GALDS) requires three distinct components: a novel bidirectional asynchronous FIFO to communicate between independently-clocked synchronous blocks [3], an all-digital dynamic clock generator to quickly an ...

Keywords: all-digital clock generation, asynchronous design, dynamic clock manager, globally asynchronous locally synchronous system

11 System architectures for computer music
John W. Gordon
June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Full text available: ⬚ pdf(4.61 MB)   Additional Information: full citation, abstract, references, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

12 The optimal logic depth per pipeline stage is 6 to 8 FO4 inverter delays
M. S. Hrishikesh, Doug Burger, Norman P. Jouppi, Stephen W. Keckler, Keith I. Farkas, Premkishore Shivakumar
May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2

Full text available: ⬚ pdf(1.03 MB) ⬚   Additional Information: full citation, abstract, references, citings, index terms
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Microprocessor clock frequency has improved by nearly 40% annually over the past decade. This improvement has been provided, in equal measure, by smaller technologies and deeper pipelines. From our study of the SPEC 2000 benchmarks, we find that for a high-performance architecture implemented in 100nm technology, the optimal clock period is

approximately 8 fan-out-of-four (FO4) inverter delays for integer benchmarks, comprised of 6 FO4 of useful work and an overhead of about 2 FO4. The optimal c ...

Keywords: Pipelining, instruction queue clock rate

13 Adaptive hybrid clock discipline algorithm for the network time protocol
David L. Mills
October 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 5
Full text available: pdf(163.51 KB)   Additional Information: full citation, references, citings, index terms

Keywords: clock discipline algorithm, computer network time synchronization, feedback control loop, oscillator error modeling

14 Improved algorithms for synchronizing computer network clocks
David L. Mills
October 1994 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Communications architectures, protocols and applications,** Volume 24 Issue 4
Full text available: pdf(1.37 MB)   Additional Information: full citation, abstract, references, citings, index terms

The Network Time Protocol (NTP) is widely deployed in the Internet to synchronize computer clocks to each other and to international standards via telephone modem, radio and satellite. The protocols and algorithms have evolved over more than a decade to produce the present NTP Version 3 specification and implementations. Most of the estimated deployment of 100,000 NTP servers and clients enjoy synchronization to within a few tens of milliseconds in the Internet of today.This pape ...

15 Improved algorithms for synchronizing computer network clocks
David L. Mills
June 1995 **IEEE/ACM Transactions on Networking (TON)**, Volume 3 Issue 3
Full text available: pdf(1.16 MB)   Additional Information: full citation, references, citings, index terms, review

16 Group F: synchronization: Adaptive clock synchronization in sensor networks
Santashil PalChaudhuri, Amit Kumar Saha, David B. Johnson
April 2004 **Proceedings of the third international symposium on Information processing in sensor networks**
Full text available: pdf(176.03 KB)   Additional Information: full citation, abstract, references, index terms

Recent advances in technology have made low cost, low power wireless sensors a reality. Clock synchronization is an important service in any distributed system, including sensor network systems. Applications of clock synchronization in sensor networks include data integration in sensors, sensor reading fusion, TDMA medium access scheduling, and power mode energy saving. However, for a number of reasons, standard clock synchronization protocols are unsuitable for direct application in sensor netw ...

Keywords: clock synchronization, probabilistic algorithms, sensor networks

17 Robust interfaces for mixed-timing systems with application to latency-insensitive protocols
Tiberiu Chelcea, Steven M. Nowick
June 2001 **Proceedings of the 38th conference on Design automation**
Additional Information:

Full text available: 📄 pdf(124.41 KB)   full citation, abstract, references, citings, index terms

This paper presents several low-latency mixed-timing FIFO designs that interface systems on a chip working at different speeds. The connected systems can be either synchronous or asynchronous. The design are then adapted to work between systems with very long interconnection delays, by migrating a single-clock solution by Carloni et al. (for "latency-insensitive" protocols) to mixed-timing domains. The new designs can be made arbitrarily robust with regard to metastability and i ...

18 Trunking of TDM and narrowband services over IP Networks   ▭

James Aweya
January 2003 **International Journal of Network Management**, Volume 13 Issue 1

Full text available: 📄 pdf(418.58 KB)   Additional Information: full citation, abstract, references, citings, index terms

The recent interest in IP as the vehicle for transporting TDM and narrowband services stems from the possibility of using a common transport network for voice, video, and data, and the flexibility with which new services can be introduced. A key step in the evolution of networks towards a 'broadband' IP-based environment is the 'graceful' interworking of the IP networks with the existing networks and services, particularly with the circuit switched telephone network. A &I ...

19 A codesign virtual machine for hierarchical, balanced hardware/software system modeling   ▭

JoAnn M. Paul, Simon N. Peffers, Donald E. Thomas
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: 📄 pdf(164.21 KB)   Additional Information: full citation, abstract, references, citings, index terms

The Codesign Virtual Machine (CVM) is introduced as a next generation system modeling semantic. The CVM permits unrestricted system-wide software and hardware behaviors to be designed to a single scheduling semantic by resolving time-based (resource) and time-independent (state-interleaved) models of computation. CVM hierarchical relationships of bus and clock state domains provide a means of exploring hardware/software scheduling trade-offs to a consistent semantic model using top-down, bo ...

20 Flow synchronization protocol   ▭

Julio Escobar, Craig Partridge, Debra Deutsch
April 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 2

Full text available: 📄 pdf(1.26 MB)   Additional Information: full citation, references, citings, index terms, review

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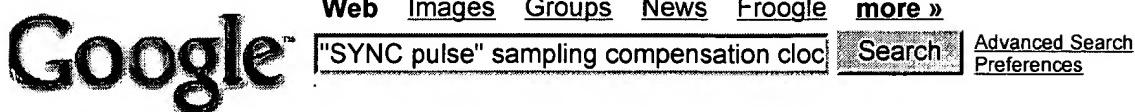
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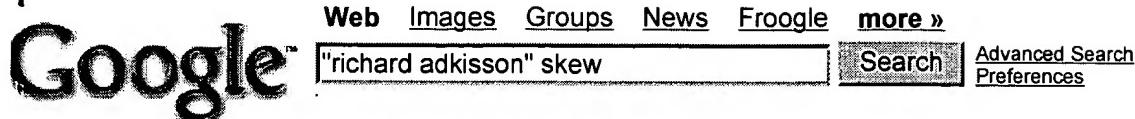
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order to show you the most relevant results, we have omitted some entries very similar to the 25 already
displayed.
you like, you can repeat the search with the omitted results included.

"SYNC pulse" sampling compens   Search

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Google | "SYNC pulse" "sampling compensation" | Search | Advanced Search
Preferences

Web
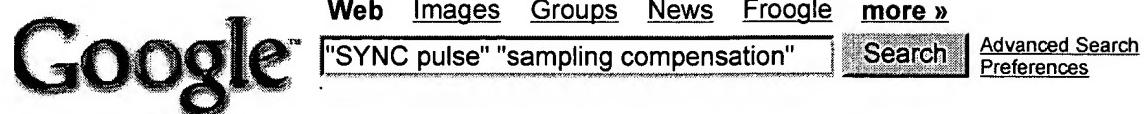
Tip: Try removing quotes from your search to get more results.

Your search - **"SYNC pulse" "sampling compensation"** - did not match any documents.

Suggestions:

- Make sure all words are spelled correctly.
- Try different keywords.
- Try more general keywords.
- Try fewer keywords.

Also, you can try Google Answers for expert help with your search.

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